Claims

We claim:

1. An integrated circuit device, comprising:

a delay circuit that is configured to delay a clock signal and is further configured to generate an output data signal in response to the delayed clock signal and an input data signal; and

a plurality of devices that are configured to respectively receive the output data signal in response to the clock signal.

2. The integrated circuit device of Claim 1, wherein the delay circuit comprises:

a memory unit that is configured to store delay information therein;

a delay buffer that is coupled to the memory unit and is configured to generate the delayed clock signal at an output terminal thereof in response to the delay information and the clock signal received at an input terminal thereof.

3. The integrated circuit device of Claim 2, wherein the delay buffer comprises:

a plurality of buffers; and

a plurality of switches that are respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

4. The integrated circuit device of Claim 3, wherein the delay circuit further comprises:

a demultiplexer circuit that couples the memory unit to the delay buffer and is configured to generate a plurality of switch control signals, respective ones of the plurality of switches being responsive to the respective ones of the plurality of switch control signals.

5. The integrated circuit device of Claim 2, wherein the delay circuit further comprises:

a receiver circuit that is configured to store the input data signal and to generate the output data signal in response to the delayed clock signal and the stored input data signal.

6. The integrated circuit of Claim 5, further comprising:

an input terminal that is coupled to both the receiver circuit and the memory unit and is configured to receive the input data signal and the delay information therethrough.

7. The integrated circuit device of Claim 1, wherein the plurality of devices comprises memory devices.

8. The integrated circuit device of Claim 1, further comprising:

a clock generation circuit that is configured to generate the clock signal in response to an input clock signal.

9. The integrated circuit device of Claim 8, wherein the clock generation circuit is a phase locked loop circuit.

10. The integrated circuit device of Claim 8, respective ones of the plurality of devices have different respective delays associated therewith with respect to receiving the output data signal.

11. An integrated circuit device, comprising:

a delay circuit that is configured to receive an input data signal in response to a clock signal and is further configured to generate an output data signal by delaying the input data signal; and

a plurality of devices that are configured to respectively receive the output data signal in response to the clock signal.

12. The integrated circuit device of Claim 11, wherein the delay circuit comprises:

a memory unit that is configured to store delay information therein;

a delay buffer that is coupled to the memory unit and is configured to generate the output data signal at an output terminal thereof in response to the delay information and the input data signal received at an input terminal thereof.

13. The integrated circuit device of Claim 12, wherein the delay buffer comprises:

a plurality of buffers; and

a plurality of switches that are respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

14. The integrated circuit device of Claim 13, wherein the delay circuit further comprises:

a demultiplexer circuit that couples the memory unit to the delay buffer and is configured to generate a plurality of switch control signals, respective ones of the plurality of switches being responsive to the respective ones of the plurality of switch control signals.

15. The integrated circuit device of Claim 12, wherein the delay circuit further comprises:

a receiver circuit that is configured to store the input data signal in response to the clock signal.

16. The integrated circuit of Claim 15, further comprising:

an input terminal that is coupled to both the receiver circuit and the memory unit and is configured to receive the input data signal and the delay information therethrough.

17. The integrated circuit device of Claim 11, wherein the plurality of devices comprises memory devices.

18. The integrated circuit device of Claim 11, further comprising:

a clock generation circuit that is configured to generate the clock signal in response to an input clock signal.

19. The integrated circuit device of Claim 18, wherein the clock generation circuit is a phase locked loop circuit.

20. An integrated circuit device, comprising:

a plurality of delay circuits that are respectively configured to delay a clock signal so as to generate a plurality of output clock signals having differing phases;

a storage circuit that is configured to generate an output data signal in response to an input data signal and one of the plurality of output clock signals; and

a plurality of devices that are configured to respectively receive the output data signal in response to respective other ones of the plurality of output clock signals.

21. The integrated circuit device of Claim 20, wherein a respective one of the plurality of delay circuits comprises:

a memory unit that is configured to store delay information therein;

a delay buffer that is coupled to the memory unit and is configured to generate a respective one of the plurality of output clock signals at an output terminal thereof in response to the delay information and the clock signal received at an input terminal thereof.

22. The integrated circuit device of Claim 21, wherein the delay buffer comprises:

a plurality of buffers; and

a plurality of switches that are respectively operable to connect selected ones of the plurality of buffers in series between the input terminal and the output terminal of the delay buffer.

23. The integrated circuit device of Claim 22, wherein the delay circuit further comprises:

a demultiplexer circuit that couples the memory unit to the delay buffer and is configured to generate a plurality of switch control signals, respective ones of the

plurality of switches being responsive to the respective ones of the plurality of switch control signals.

24. The integrated circuit device of Claim 20, wherein the plurality of devices comprises memory devices.

25. The integrated circuit device of Claim 20, further comprising:

a clock generation circuit that is configured to generate the clock signal in response to an input clock signal.

26. The integrated circuit device of Claim 25, wherein the clock generation circuit is a phase locked loop circuit.

27. A method of operating an integrated circuit device, comprising:

storing delay information in a memory unit;

delaying a clock signal based on the delay information;

generating an output data signal in response to the delayed clock signal and an input data signal; and

receiving the output data signal at a plurality of devices in response to the clock signal.

28. The method of Claim 27, wherein generating the output data signal comprises:

storing the input data signal;

generating the output data signal in response to the delayed clock signal and the stored input data signal.

29. A method of operating an integrated circuit device, comprising:

storing delay information in a memory unit;

receiving an input data signal in response to a clock signal;

delaying the input data signal based on the delay information to generate an output data signal; and

receiving the output data signal at a plurality of devices in response to the clock signal.

30. A method of operating an integrated circuit device, comprising:

generating a plurality of output clock signals having differing phases by applying different delays to a clock signal;

generating an output data signal in response to an input data signal and one of the plurality of output clock signals; and

receiving the output data signal at respective ones of a plurality of devices in response to respective other ones of the plurality of output clock signals.

31. The method of Claim 30, further comprising:

storing delay information in a memory unit; and

wherein generating the plurality of output clock signals comprises generating the plurality of output clock signals having differing phases by applying different delays based on the delay information to the clock signal.